LIGHT RECEIVING CIRCUIT AND OPTICAL COUPLING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-050045, filed March 12, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a light receiving circuit and a optical coupling device.

BACKGROUND

A optical coupling element, an optical communication device, and the like are widely used for various electronic apparatuses for industry, communication, and home. These days, for a light emission element which is used for the apparatuses, light emission efficiency is improving.

Intensity of a light signal which is handled in the light receiving circuit includes intensity from a weak level to an extremely strong level, and a light receiving circuit with a wide dynamic range is demanded.

An example of related art includes JP-A-2009-88580.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating a light receiving circuit according to a first embodiment.

FIG. 2 is a circuit diagram of a light receiving circuit in which the circuit of FIG. 1 is illustrated as a more specific circuit element.

FIG. 3 is a circuit diagram of a light receiving circuit of a comparison example.

FIG. 4A is a graph representing frequency characteristics of a light receiving circuit according to the present embodiment. FIG. 4B is a graph representing frequency characteristics of a light receiving circuit of a comparison example.

FIG. 5 is a graph that represents pulse response characteristics of a light receiving circuit according to the present embodiment in comparison with pulse response characteristics of a light receiving circuit of a comparison example.

FIG. 6 is a circuit diagram illustrating a light receiving circuit according to a second embodiment.

FIG. 7 is a circuit diagram illustrating a light receiving circuit according to a third embodiment.

FIG. 8 is a graph that represents by comparing pulse response characteristics of a light receiving circuit according to the present embodiment with pulse response characteristics of a light receiving circuit according to another embodiment.

FIG. 9 is a circuit diagram illustrating a light receiving circuit according to a fourth embodiment.

FIG. 10A is a block diagram illustrating an optical coupling device according to a fifth embodiment. FIG. 10B is a sectional diagram illustrating a structure of the optical coupling device according to the fifth embodiment.

FIG. 11 is a block diagram illustrating an optical communication system according to a sixth embodiment.

DETAILED DESCRIPTION

[0005]

Exemplary embodiments provide a light receiving circuit and an optical coupling device which maintain frequency characteristics and operate at a low voltage.

[0006]

A light receiving circuit according to an embodiment includes a light receiving element; a first MOS transistor of a first conductive type that includes a first gate electrode which is coupled to the light receiving element, a first source electrode which is coupled to a reference potential line, and a first drain electrode which is coupled to a first load circuit via a first node, and can operate in a saturation region; a second MOS transistor of a second conductive type that includes a second gate electrode which is coupled to the first node, a second source electrode which is coupled to an output terminal, and a second drain electrode which is coupled to the reference potential line; a second load circuit that is coupled between a power supply potential line and the second drain electrode; and a feedback resistor element that is coupled between the first gate electrode and the output terminal.

[0008]

Hereinafter, exemplary embodiments will be described with reference to the drawings.

First Embodiment

FIG. 1 is a circuit diagram illustrating a light receiving circuit according to a first embodiment.

FIG. 2 is a circuit diagram of a light receiving circuit in which the circuit of FIG. 1 is illustrated as a more specific circuit element.

FIG. 3 is a circuit diagram of a light receiving circuit of a comparison example.

FIG. 4A is a graph representing frequency characteristics of a light receiving circuit according to the present embodiment. FIG. 4B is a graph representing frequency characteristics of a light receiving circuit of a comparison example.

FIG. 5 is a graph that represents pulse response characteristics of a light receiving circuit according to the present embodiment in comparison with pulse response characteristics of a light receiving circuit of a comparison example.

As illustrated in FIG. 1, a light receiving circuit 10 according to the present embodiment includes a light receiving element 1, an amplification transistor 1, an output transistor 2, a load circuit 13, and a feedback resistor element 14. The light receiving circuit 10 is coupled between a power supply terminal 15 and a reference voltage terminal 16. A potential Vss of the reference voltage terminal 16 is the lowest potential among potentials which are coupled to the light receiving circuit 10, is typically a ground potential, and is 0 V. A potential Vdd of the power supply terminal 15 is the highest potential among potentials which are coupled to the light receiving circuit 10, and is, for example, 2.5 V with respect to the ground potential. For the potential Vss of the reference voltage terminal 16 and the potential Vdd of the power supply terminal 15, it is better if the above-described potential relationship is maintained. Both or one of the potential Vss of the reference voltage terminal 16 and the potential Vdd of the power supply terminal 15 may be a negative potential.

[0009]

In the present specification, it is assumed that a saturation region of a MOS transistor indicates a region in which a drain current (output current) is proportional to square of a voltage difference between a gate-source voltage and a threshold voltage, in output characteristics between a drain and ×a source of a MOS transistor. More specifically, a drain current Id in a saturation region is represented as follows.

[0010]

Id=(k/2)´(Vg-Vt)2 (1)

Here, Vg is a gate-source voltage of a MOS transistor, and Vt is a gate threshold voltage of a MOS transistor. In addition, k is represented by k=(W/L)×m×Cox. W and L are respectively a gate width and a gate length of a MOS transistor. m is mobility of a carrier (electron if n-channel, hole if p-channel) in a channel, and Cox is a capacitance which is generated by a gate oxide film.

[0011]

A drain current represents approximately a constant value with respect to a drain-source voltage, in a saturation region of a MOS transistor. In contrast to this, a linear region of a MOS transistor is a region in which a drain current has a linear term of a drain-source voltage which includes a voltage difference between a gate-source voltage and a threshold voltage in a proportionality constant, in output characteristics of a MOS transistor. More specifically, the drain current Id in a saturation region is represented as follows.

[0012]

Id=k´{(Vg-Vt)´Vd-(1/2)´Vd2} (2)

Here, Vd is a drain-source voltage of a MOS transistor, and the other parameters are the same as the parameters in expression (1).

[0013]

A drain-source voltage in a boundary between a saturation region and a linear region of a MOS transistor is equal to a voltage difference between a gate-source voltage and a threshold voltage, and a drain-source voltage at this time may be referred to as an overdrive voltage. It is assumed that saturation of an output waveform or the like indicates a case or the like in which a voltage waveform having a waveform that is different from an expected output voltage waveform, for example, a distorted waveform is represented, as a MOS transistor related to an output voltage waveform operates at a linear region, in an output voltage waveform of a light receiving circuit.

[0014]

In addition, a threshold voltage of a p-channel MOS transistor is represented in general by a negative value, but it is assumed that, in the present specification, representation of an absolute value is omitted, the threshold value is treated as a positive value, while not being particularly limited.

[0015]

The light receiving element 11 is coupled between the reference voltage terminal 16 and an input node 18. The light receiving element 11 is, for example, a silicon photodiode. The light receiving element 11 may be a photoelectric conversion element such as a silicon PIN photodiode or an avalanche photodiode, according to a light transmission distance, communication speed, or the like, in addition to the silicon photodiode. In addition, the light receiving element 11 may be a photodiode which uses a semiconductor material other than silicon.

[0016]

The amplification transistor (first MOS transistor) 1 includes a gate electrode 1a which is coupled to the light receiving element 11 by the input node 18, a source electrode 1b which is coupled to the reference potential Vss, and a drain electrode 1c which inverts a voltage that is input to the gate electrode 1a and outputs the inverted voltage. The drain electrode 1c of the amplification transistor 1 is directly coupled to a load circuit 12 by an internal output node 19 (first node). The amplification transistor 1 is, for example, an n-channel MOSFET.

[0017]

The amplification transistor 1 is coupled in series to the load circuit 12. The load circuit 12 is configured by a current source having a current value I1. The load circuit 12 is coupled between the power supply potential Vdd and the internal output node 19.

[0018]

The amplification transistor 1 configures a source ground amplification circuit in which an operation point is set by the load circuit 12. Setting of an operation point of a MOS transistor means setting of a drain current in the saturation region of the MOS transistor. In other words, it means that a current value of the load circuit is set in such a manner that a desired drain current of the MOS transistor flows, according to expression (1) described above.

[0019]

The output transistor (second MOS transistor) 2 includes a gate electrode 2a which is coupled to the drain electrode 1c of the amplification transistor 1 by the internal output node 19, a source electrode 2b which is coupled to the load circuit 13 and an output terminal 17 by an output node 20, and a drain electrode 2c which is coupled to the reference potential Vss. The output transistor 2 is a MOS transistor of a conductive type which is different from the amplification transistor 1, and is a p-channel MOSFET if the amplification transistor 1 is an n-channel MOSFET. In an operation state of the light receiving circuit 10, an absolute value Vgs2 of a gate-source voltage of the output transistor 2 is smaller than a threshold voltage Vth1 of the amplification transistor 1. The output transistor 2 is configured by an n-channel MOSFET if the amplification transistor 1 is a p-channel MOSFET. A potential of the source electrode 2b of the output transistor 2 is changed by an output signal, and thereby a back gate electrode 2d is coupled to a source electrode 2b.

[0020]

The load circuit 13 is configured by a current source having a current value I2. The load circuit 13 is coupled between the power supply potential Vdd and an output node 20 to which the output terminal 17 and the source electrode 2b of the output transistor 2 are coupled.

[0021]

The output transistor 2 is coupled in series to the load circuit 13. The output transistor 2 is a source follower circuit in which an operation point is set by the load circuit 13. The source follower circuit which includes the output transistor 2 and the load circuit 13, is an output circuit which receives an output of a source ground amplification circuit that includes the amplification transistor 1 and the load circuit 12 with a high impedance, and outputs the received signal with a low impedance.

[0022]

As illustrated in FIG. 2, a current mirror circuit can be used for current sources of the load circuits 12 and 13. A transistor 21 which is diode-coupled is coupled between the power supply potential Vdd and the ground potential Vss. For the transistor 21, a current value which is used as a reference is set by a resistor element 22 which is coupled between the transistor 21 and the ground potential Vss. A current mirror 23 is coupled between the power supply potential Vdd and the internal output node 19. A current mirror 24 is coupled between the power supply potential Vdd and the internal output node 20. Each gate electrode of the current mirrors 23 and 24 is coupled to a gate electrode of the transistor 21. Current values of the current mirrors 23 and 24 are determined by the transistor 21, and a transistor size of the respective current mirrors 23 and 24. That is, if a size ratio between the transistor 21 and the respective transistors of the current mirrors 23 and 24 is, for example, 1:1:1, values of currents flowing through the respective transistors are equal to each other.

[0023]

An element which is configured by a resistor element may be used for the load circuits 12 and 13, in addition to a current source circuit which is configured by a current mirror circuit or the like.

[0024]

The feedback resistor element 14 is coupled between the input node 18 and the output node 20. Thus, the light receiving circuit 10 includes a transimpedance amplification circuit TIA in which the feedback resistor element 14 is coupled between an input and an output of an inversion amplification circuit that is configured by a source ground amplification circuit and a source follower circuit which are cascaded to each other.

[0025]

The transimpedance amplification circuit TIA inputs an output current which is output according to an amount of light received by the light receiving element 11, converts the current into a voltage, and outputs the voltage.

[0026]

Next, an operation of the light receiving circuit according to the present embodiment will be described using FIG. 2.

It is assumed that the reference potential Vss is a ground potential and is 0 V. Thus, the power supply voltage is equal to the power supply potential Vdd.

[0027]

To begin with, a case of no signal will be described. No signal in the light receiving circuit 10 means that there is no light irradiation into the light receiving element 11 and the light receiving element 11 does not generate an output current. It is assumed that a current which is generated by a dark current or the like of the light receiving element 11 is disregarded.

[0028]

At the time of no signal, the light receiving element 11 does not output a current, and thus a voltage drop does not occur in both ends of the feedback resistor element 14. For this reason, a voltage Vout of the output node 20 is equal to a voltage of the input node 18, that is, a gate-source voltage Vgs1 of the amplification transistor 1.

[0029]

The drain electrode 1c of the amplification transistor 1 is coupled to the gate electrode 2a of the output transistor 2, and thus a drain-source voltage Vds1 of the amplification transistor 1 is determined by a gate-source voltage Vgs2 of the output transistor 2. More specifically, the drain-source voltage Vds1 of the amplification transistor 1 is equal to a difference between the voltage Vout of the output node 20 and the gate-source voltage Vgs2 of the output transistor (Vds1=Vout-Vgs2=Vgs1-Vgs2). The gate-source voltage Vgs2 of the output transistor 2 is determined by expression (1) in such a manner that the current value I2 of the current mirror 24 is set to the drain current Id2.

[0030]

Even if the drain-source voltage Vds1 is decreased to the overdrive voltage Vov1, the amplification transistor 1 can operate in a saturation region. That is, the drain-source voltage Vds1 needs to be equal to or higher than the overdrive voltage Vov1. That is, when Vds1³Vov1 is satisfied, the amplification transistor 1 operates in the saturation region. In addition, as described above, Vds1=Vgs1-vgs2 is satisfied and thereby the following expression is obtained.

[0031]

Vgs1-Vgs2³Vov1

[0032]

Here, if Vgs1 is removed by Vov1=Vgs1-Vth1, the following expression is obtained.

[0033]

Vov1+Vth1-Vgs2³Vov1

\Vth1³Vgs2 (3)

[0034]

Here, Vth1 is a threshold voltage of the amplification transistor 1. Vov1 is an overdrive voltage of the amplification transistor 1. The overdrive voltage Vov1 is equal to a difference between the gate-source voltage Vgs1 and the threshold voltage Vth1.

[0035]

The amplification transistor 1 operates at a saturation region by expression (1) and expression (3). The gate-source voltage Vgs1 at this time is equal to the threshold voltage Vth1 or a voltage higher than the threshold voltage Vth1, and is a voltage value by which the drain current Id1 that is approximately equal to the current value I1 of the current mirror 23 flows (expression (1)).

[0036]

Next, when the light receiving element11 receives light and outputs a current, an operation of the light receiving circuit 10 will be described. The light receiving element 11 receives light and generates an output current according to an amount of light. A current which is output from the light receiving element 11 flows toward the input node 18 from the output node 20 via the feedback resistor element 14. The voltage Vout of the output node 20 is increased by a voltage drop which is generated by the feedback resistor element 14 according to a current flowing through the feedback resistor element 14. That is, the output voltage Vout of the light receiving circuit becomes a voltage which is nearly proportional to an output current that is generated by the light receiving element 11. Thus, the light receiving circuit 10 outputs a maximum voltage when light is irradiated into the light receiving element 11 and light receiving element 11 outputs a current. A maximum output voltage is calculated as follows.

[0037]

As an output voltage of the light receiving circuit 10 increases, a voltage between the power supply terminal 15 and the output terminal 17 is decreased. A voltage between the power supply terminal 15 and the output terminal 17 is applied to both ends of the current mirror 24, and thereby a maximum value of the output voltage is determined by a condition in which the current mirror 24 deviates from the saturation region. That is, when a voltage between both ends of the current mirror 24 is equal to an overdrive voltage Vov24, the output voltage becomes maximum. The overdrive voltage Vov24 of the current mirror 24 is a difference between a gate-source voltage Vgs24 of the current mirror 24 and a threshold voltage Vth24, and thus Vov24=Vgs24-Vth24. A voltage as high as a gate-source voltage of the output transistor 2 is applied between a drain and a source of the current mirror 23 and between a drain and a source of the current mirror 24. For this reason, the current mirror 24 deviates from the saturation region prior to the current mirror 23. Thus, the maximum output voltage Vout(max) is represented by the following expression.

[0038]

Vout(max)=Vdd-Vov24 (4)

[0039]

The gate-source voltage Vgs2 of the output transistor 2 is approximately a constant value which is determined by a current that is set by the current mirror 24.

[0040]

The gate electrode 2a of the output transistor 2 is coupled to the drain electrode 1c of the amplification transistor 1. For this reason, the drain-source voltage Vds1 of the amplification transistor 1 is equal to a value which is obtained by subtracting the gate-source voltage Vgs2 of the output transistor 2 from the voltage Vout of the output node 20. The gate-source voltage Vgs2 is set by a current which is set by the current mirror 24, and is approximately a constant value. As described above, the voltage Vout of the output node 20 is a voltage higher than a voltage at the time of no signal, and the gate-source voltage Vgs2 is nearly constant, and thus the drain-source voltage Vds1 of the amplification transistor 1 is higher than the overdrive voltage Vov1. Thus, when there is a signal, the amplification transistor 1 is guaranteed to operate in the saturation region. If a resistor element or the like is used instead of a current mirror as a load circuit, there are no overdrive voltage restrictions, and thereby it is possible to reduce a voltage which can be applied to both ends of a load circuit. Thus, it is possible to increase a maximum output voltage of the light receiving circuit 10.

[0041]

Next, an operation and an effect of light receiving circuit 10 according to the present embodiment will be described while light receiving circuit 10 is compared with a light receiving circuit of a comparison example.

[0042]

As illustrated in FIG. 3, a light receiving circuit 100 of a comparison example is different from the light receiving circuit 10 according to the above-described embodiment in that an output transistor 102 is an n-channel MOSFET of a conductive type which is the same as an amplification transistor 101, and the light receiving circuit 100 is a source follower which uses a load circuit 113 as a load. That is, the output transistor 102 is coupled between the power supply potential Vdd and an output node 120, and the load circuit 113 is coupled between the output node 120 and the reference potential Vss.

[0043]

In the light receiving circuit 100 of the comparison example, as a minimum output voltage Vout0’ at the time of no signal, a gate-source voltage Vgs101 of the amplification transistor 101 is output, in the same manner as light receiving circuit 10 according to the first embodiment. In light receiving circuit 100 of the comparison example, at the time of no signal, a MOS transistor which moves from a saturation region to a linear region does not exists, and thereby Vout0’=Vgs101 without a special condition.

[0044]

When there is a signal, a maximum output voltage Vout(max)’ is obtained as follows.

In the light receiving circuit 100 of the comparison example, if the maximum output voltage Vout(max)’ is output, the output transistor 102 configures a source follower, and thereby the output voltage Vout increases, and a potential of a gate electrode of the output transistor 102 increases. Thus, a current mirror 112 which is coupled between the power supply potential Vdd and a gate electrode of the output transistor 102 may deviate from a saturation region.

[0045]

When the current mirror 112 moves from a saturation region to a linear region, if a voltage between both ends of the current mirror 112 is referred to as Vov112 and a gate-source voltage of the output transistor 102 is referred to as Vgs102, the maximum output voltage Vout(max)’ is obtained by the following expression.

[0046]

Vout(max)’=Vdd-Vov112-Vgs102 (5)

[0047]

For example, in expression (5), if the power supply potential Vdd is set to 2.5 V, the overdrive voltage Vov112 of the current mirror 112 is set to 0.4 V, a transistor with a low threshold is used as the output transistor 102, and Vgs102 is set to 0.5 V, the following expression is obtained.

Vout(max)’=2.5 V-0.4 V-0.5 V=1.6 V

[0048]

Meanwhile, in a case of light receiving circuit 10 according to the present embodiment, at the time of no signal, an output current is zero without light irradiation into light receiving element 11. Thus, the voltage Vout of the output node 20 is equal to a voltage of the input node 18, that is, the gate-source voltage Vgs1 of the amplification transistor 1. An output voltage at this time is a minimum output voltage Vout0 of light receiving circuit 10 according to the present embodiment. The gate-source voltage Vgs1 is determined by a drain current which is set by the load circuit 12 that determines an operation point, and can be set to 1 V in the same manner as a case of light receiving circuit 100 of the comparison example, for example.

[0049]

At this time, a relationship of expression (3) needs to be satisfied between the threshold voltage Vth1 of the amplification transistor 1 and the gate-source voltage Vgs2 of the output transistor 2. Expression (3) is as follows if rewritten.

[0050]

Vth1³Vgs2 (3)

[0051]

Thus, the magnitude of a minimum output voltage satisfies a condition of expression (3), and thereby the light receiving circuit 10 according to the present embodiment can realize the same value as the minimum output voltage of the light receiving circuit 100 of the comparison example.

[0052]

As described above, when there is a signal, the maximum output voltage Vout(max) the light receiving circuit 10 according to the present embodiment is equal to a voltage which is obtained by subtracting a minimum voltage of both ends of the current mirror 24 from the power supply voltage Vdd. Expression (4) representing the maximum output voltage Vout(max) of the light receiving circuit 10 is as follows, if rewritten.

[0053]

Vout(max)=Vdd-Vov24 (4)

If the power supply voltage Vdd=2.5 V and Vov24=0.4 V, the following expression is obtained by using expression (4).

Vout(max)=2.5 V-0.4 V=2.1 V

[0054]

As described above, a maximum output voltage Vout(max)’ of light receiving circuit 100 of the comparison example is 1.6 V, and in the light receiving circuit 10 according to the present embodiment, a higher output voltage can be obtained.

[0055]

As described above, a dynamic range of light receiving circuit 10 according to the first embodiment 2.1 V-1 V=1.1 V, and in contrast to this, a dynamic range of light receiving circuit 100 of the comparison example 1.6 V-1 V=0.6 V. In the light receiving circuit 100 of the comparison example, the gate-source voltage Vgs102 of the output transistor 102 is coupled in series in addition to a load circuit of one stage. In contrast to this, in the light receiving circuit 10 according to the present embodiment, a load circuit of the current mirror 24 or the like of only one stage is coupled between the power supply terminal 15 and the output terminal 17 (output node 20). For this reason, it is possible to reduce a voltage between the power supply terminal 15 and the output terminal 17, and thereby the light receiving circuit 10 can output a higher output voltage.

[0056]

In addition, in the light receiving circuit 10 according to the present embodiment, a voltage between the power supply terminal 15 and the output terminal 17 can be reduced to a lower voltage, and thereby it is possible to increase a voltage which is applied between drains and sources of the amplification transistor 1 and the output transistor 2. For this reason, it is possible to improve frequency characteristics of the amplification transistor 1 and the output transistor 2, and to improve power supply voltage dependence of small signal frequency characteristics and pulse response characteristics of the light receiving circuit 10, as described below.

[0057]

As illustrated in FIG. 4A, in the light receiving circuit 10 according to the present embodiment, even if the power supply voltage Vdd is 1.75 V and even if the power supply voltage Vdd is 1.25 V, frequency characteristics are nearly not changed. Meanwhile, as illustrated in FIG. 4B, in the light receiving circuit 100 of the comparison example, if the power supply voltage Vdd is 1.75 V, the frequency characteristics thereof nearly does not have a difference with the frequency characteristics of light receiving circuit 10 according to the present embodiment, but if the power supply voltage Vdd is 1.25 V, the frequency characteristics are significantly degraded.

[0058]

As illustrated in FIG. 5, in the light receiving circuit 10 according to the present embodiment, frequency characteristics of a large amplitude, that is, pulse response characteristics also hardly generate saturation of an output waveform, compared to the light receiving circuit 100 of the comparison example, and approximately the same output voltage as that of the light receiving circuit 100 is obtained in the input current waveform (graph of a solid line). Meanwhile, in the light receiving circuit 100 of the comparison example, since a dynamic range is narrow, a pulse width in which an output waveform is distorted is formed so as to be wider than a pulse width of an output current of the light receiving element 11 (graph of a dashed line). In the pulse response characteristics of FIG. 5, the power supply voltage Vdd is set to 2. 5V, and resistance values of the feedback resistor elements 14 and 114 are set to 50 kW. In addition, a maximum output current of the light receiving element is set to 25 mA.

[0059]

As described above, in the light receiving circuit 10 according to the present embodiment, the output transistor 2 uses a source follower circuit using a MOS transistor with a polarity different from that of the amplification transistor, a p-channel MOS transistor in the example described above. For this reason, the light receiving circuit 10 also allows an increase of an output voltage which is determined by a load circuit of a source follower. Meanwhile, in the light receiving circuit 10 according to the present embodiment, the gate electrode 2a of the output transistor 2 is coupled to the drain electrode 1c of the amplification transistor 1, and design parameters of the amplification transistor 1 and the output transistor 2 are set so as to satisfy the conditions of expression (3). For this reason, the drain-source voltage Vds1 of the amplification transistor 1 operates at a voltage equal to or higher than the overdrive voltage Vov1, and an operation in the saturation region of the amplification transistor 1 is guaranteed. Thus, in the light receiving circuit 10 according to the present embodiment, a dynamic range is wide.

[0060]

These days, low power consumption of a device is strongly demanded, and for this reason, a low voltage operation is demanded for a component or an element which configures a device. In the light receiving circuit 10 according to the present embodiment, a low voltage can be applied to an output load circuit 13, and thereby there is room for a voltage range in which the amplification transistor 1 and the output transistor 2 can operate. For this reason, even if a power supply is decreased, it is possible to reduce degradation of frequency characteristics and pulse response characteristics. Thus, in the light receiving circuit 10 according to the present embodiment, a lower voltage operation can be performed, and it is possible to contribute to a low power consumption of a device.

[0061]

For example, if a waveform of the output voltage Vout which is generated in the output terminal 17 of the light receiving circuit 10 is saturated and is not distorted, or the distortion is sufficiently small, there may be a case in which the amplification transistor 1 operates by containing a portion of an amplitude of an output voltage in the linear region (expression (2)). For a distortion magnitude of the waveform of the output voltage Vout, an appropriate value is set by a coupling condition or the like of a circuit in a subsequent stage. This is also applied in the same manner as in a light receiving circuit according to another embodiment which will be described hereinafter.

Second Embodiment

[0062]

FIG. 6 is a circuit diagram illustrating a light receiving circuit according to a second embodiment.

In the light receiving circuit 10 according to the first embodiment described above, the threshold voltage of the output transistor 2 is set to a value lower than the threshold voltage Vth1 of the amplification transistor 1, and the gate-source voltage Vgs2 at the time of operating the output transistor 2 is set to a voltage equal to or lower than Vth1 (expression (1)). In order to set a low threshold voltage Vth2 of the output transistor 2, it is better if fabrication parameters is set so as to fabricate a p-channel MOSFET with a low threshold voltage, in a semiconductor fabrication process. Thus, there is a case in which a p-channel MOSFET with a stably low threshold voltage is hardly fabricated by a threshold voltage. In addition, in order to fabricate a transistor with various types of threshold voltages, the number of fabrication processes is increased and cost is also increased. Therefore, by applying a voltage to a back gate electrode of a p-channel MOSFET from the outside, the threshold voltage is shifted, and a p-channel MOSFET with actually low threshold voltage is formed.

[0063]

As illustrated in FIG. 6, a light receiving circuit 10a according to the present embodiment further includes a resistor element 8 for setting a threshold voltage, and a power supply (second power supply) 9 for setting a threshold voltage. The resistor element 8 is coupled between the source electrode 2b of the output transistor 2 and the back gate electrode 2d. The power supply 9 is coupled between the back gate 2d and the reference potential Vss. The power supply 9 makes a constant current with a current value I9 flow through the resistor element 8, and thereby a voltage is generated on both ends of the resistor element 8. A voltage is applied to both ends of the resistor element 8, in such a manner that a forward bias is applied between the source electrode 2b of the output transistor 2 and the back gate electrode 2d. The voltage which is applied between the source electrode 2b of the output transistor 2 and the back gate electrode 2d is (resistance value R8 of the resistor element 8)´(current value I9 of the power supply 9). As a potential of the back gate electrode 2d is lower than a potential of the source electrode 2b by R8´I9, the threshold voltage Vth2’ of the output transistor 2 is set to a low voltage value.

[0064]

The resistor element 8 and the power supply 9 for setting a threshold voltage are provided, and thereby the output transistor 2 can stably generate a threshold voltage lower than the threshold voltage Vth1 of the amplification transistor 1, without a fabrication process being added. Thus, it is possible to easily realize the light receiving circuit 10a with a wide dynamic range.

Third Embodiment

[0065]

FIG. 7 is a circuit diagram illustrating a light receiving circuit according to a third embodiment.

FIG. 8 is a graph that represents pulse response characteristics of the light receiving circuit according to the present embodiment and pulse response characteristics of the light receiving circuit according to a the first embodiment by comparison.

In a light receiving circuit, in order to widen a dynamic range of an output, it is necessary to be able to input an output current which is output by a light receiving element, over a wide range. If light with a weak level is received and light with a sufficient level is intended to be output, when a strong light is received, a load circuit of an output circuit deviates from a saturation region and moves to a linear region. For this reason, an output signal waveform is crushed and thereby a voltage signal with a pulse width different from a pulse width of an input signal waveform is output, and thus it is necessary to prevent a MOS transistor from deviating from a saturation region. Therefore, in a light receiving circuit with a wide dynamic range, an amplitude of an output signal which is output by an output circuit is limited, and a limiter circuit is added in such a manner that an output circuit does not operate in a linear region. Meanwhile, if a level of an output signal waveform is limited by adding a limiter circuit, an amount of feedback of an amplifier is changed, and a light receiving circuit can be unstable. Therefore, it is necessary to further add a circuit which secures a stable operation of a light receiving circuit at the time of limiter circuit operation, in addition to a limiter circuit.

[0066]

As illustrated in FIG. 7, the light receiving circuit 10 according to the present embodiment further includes a limiter circuit 30, a bypass circuit 40, and a voltage generation circuit 50. The other circuit elements are the same as those of the light receiving circuit 10 according to the first embodiment, the same symbols or reference numerals will be attached to the same elements, and detailed description thereof will be omitted.

[0067]

The limiter circuit 30 includes a limiter transistor 3 (third MOS transistor) and a resistor element 32. The limiter transistor 3 includes a gate electrode 3a which is coupled to the output node 20, a source electrode 3b which is coupled to one terminal of the resistor element 32, and a drain electrode 3c which is coupled to the power supply potential Vdd. The other terminal of the resistor element 32 is coupled to the input node 18. The resistor element 32 is coupled to the output node 20 via a gate-source voltage of the limiter transistor 3, and thereby the resistor element 32 is coupled substantially in parallel with the feedback resistor element 14, and a resistance value is set according to a dynamic range.

[0068]

If the light receiving element 11 receives light and output a current, the current which is output flows into the feedback resistor element 14. If an amount of light received by the light receiving element 11 is small, a current flowing through the feedback resistor element 14 is small, a voltage on both ends of the feedback resistor element 14 is smaller than a threshold voltage of the limiter transistor 3. For this reason, a potential of the output node 20 increases according to the value of a current flowing through the feedback resistor element 14. The threshold voltage of the limiter transistor 3 is set so as not to turn on the limiter transistor 3, in a range in which the load circuit 13 does not move from a saturation state to a linear region. If a current which is output from the light receiving element 11 is increased, and a voltage on both ends of the feedback resistor element 14 exceeds a threshold voltage of the limiter transistor 3, the limiter transistor 3 is turned on. If the limiter transistor 3 is turned on, an increase of a voltage of both ends of the feedback resistor element 14 is limited. For this reason, a voltage increase of the output node 20 is limited, and the load circuit 13 is prevented from moving to a linear region from a saturation region. By doing this, if a large signal is input, the limiter circuit 30 operates in such a manner that the load circuit 13 is prevented from deviating from a saturation region and a level of an output signal is not saturated.

[0069]

The bypass circuit 40 includes a resistor element 42, and a bypass transistor 4 (fourth MOS transistor) which is diode-coupled. The resistor element 42 is coupled in series to the bypass transistor 4. The bypass circuit 40 is coupled between an internal output node 19 and an output terminal 50a of a voltage generation circuit 50. The bypass transistor 4 is coupled in a direction in which a current flows toward an output terminal 50a of the voltage generation circuit 50 from the internal output node 19. The resistor element 42 sets the value of a current flowing when the bypass transistor 4 is turned on.

[0070]

The voltage generation circuit 50 includes an n-channel MOS transistor 5 (fifth MOS transistor), a p-channel MOS transistor 6 (sixth MOS transistor), and a load circuit 54. The load circuit 54, the p-channel MOS transistor 6, and the n-channel MOS transistor 5 are sequentially coupled in series, and are coupled between the power supply potential Vdd and the reference potential Vss. The load circuit 54 is coupled between the power supply potential Vdd and a source electrode 6b of the p-channel MOS transistor 6. A gate electrode 6a of the p-channel MOS transistor 6 is coupled to a drain electrode 6c, and is coupled to a drain electrode 5c of the n-channel MOS transistor 5. A gate electrode 5a of the n-channel MOS transistor 5 is coupled to the source electrode 6b of the p-channel MOS transistor 6. A source electrode 5b of the n-channel MOS transistor 5 is coupled to the reference potential Vss. The voltage generation circuit 50 outputs a potential equal to a potential of the internal output node 19 at the time of no signal from the output terminal 50a. The output terminal 50a is coupled to the drain electrode 5c of the n-channel MOSFET 5.

[0071]

The n-channel MOS transistor 5 is a MOSFET with the same polarity as that of the amplification transistor 1, and is an n-channel MOSFET, if the amplification transistor 1 is an n-channel MOSFET. If the amplification transistor 1 is a p-channel MOSFET, the MOS transistor 5 is a p-channel MOSFET. The n-channel MOS transistor 5 and the amplification transistor 1 are set in such a manner that threshold voltages thereof are approximately equal. The p-channel MOS transistor 6 is a MOSFET with the same polarity as that of the output transistor 2, and is a p-channel MOSFET, if the output transistor 2 is a p-channel MOSFET. If the output transistor 2 is an n-channel MOSFET, the MOS transistor 6 is an n-channel MOSFET. The output transistor 2 and the MOS transistor 6 are set so as to have a nearly equal value. In this way, by matching the respective threshold voltages to each other, the drain electrode 5c of the n-channel MOS transistor 5 outputs a voltage equal to a voltage of the internal output node 19 at the time of no signal.

[0072]

For example, the current values of the load circuits 12, 13, and 54 are all set so as to be equal to one another, and a transistor size of the n-channel MOS transistor 5 and a transistor size of the amplification transistor 1 are set so as to be equal to each other. In addition, a transistor size of the p-channel MOS transistor 6 and a transistor size of the output transistor 2 are set so as to be equal to each other. By setting the current values and the transistor sizes in this way, it is possible to set a transistor with uniform threshold voltage described above. Here, it is assumed that the transistor size is represented by a gate width/a gate length of a MOSFET.

[0073]

The limiter circuit 30, the bypass circuit 40, and the voltage generation circuit 50 operate as follows.

At the time of no signal, the gate-source voltage Vgs1 of the amplification transistor 1 is output from the output terminal 17. In a state in which the light receiving element 11 outputs a small output current and the limiter transistor 3 does not operate, a voltage which is obtained by doubling an output current of the light receiving element 11 by a transimpedance is output from the output terminal 17. If the threshold voltage Vth1 of the amplification transistor 1 and the gate-source voltage Vgs2 of the output transistor 2 satisfy a relationship of the above-described expression (1), the amplification transistor 1 does not deviate from a saturation region.

[0074]

If a current which is output from the light receiving element 11 is large and the limiter transistor 3 is turned on, when there is no bypass transistor 4, an equivalent feedback resistance value is decreased. A polarity which is formed by the equivalent feedback resistance value and a capacitance value between the terminals of the light receiving element 11 is formed so as to approach a polarity of an amplification circuit which is configured by the amplification transistor 1, the load circuit 12, the output transistor 2, and the load circuit 13, and thereby an amplification circuit performs an unstable operation such as an oscillation operation. In the light receiving circuit 10b according to the present embodiment, the source electrode 4b of the bypass transistor 4 is maintained as a voltage of the output terminal 50a of the voltage generation circuit 50, that is, a voltage of the drain electrode 5c of the n-channel MOS transistor 5. At this time, if the limiter transistor 3 is turned on, a potential of the internal output node 19 increases, and thereby the bypass transistor 4 is simultaneously turned on with the limiter transistor 3. As the bypass transistor 4 is turned on, a loop gain of an amplification circuit which is configured by the amplification transistor 1, the load circuit 12, the output transistor 2, and the load circuit 13 is decreased, and a stable operation of the amplification circuit is realized.

[0075]

The voltage generation circuit 50 can be configured by an arbitrary circuit which outputs a voltage equal to the internal output node 19 at the time of no signal, while not being limited to the configuration described above.

[0076]

As illustrated in FIG. 8, it can be seen that, in the light receiving circuit 10b according to the present embodiment, also in frequency characteristics of a large amplitude, that is, pulse response characteristics, crushing due to the saturation of an output waveform does not occur and an output voltage nearly equal to an input current waveform is obtained (graph of a solid line), compared to the light receiving circuit 10 (graph of an alternate long and short dash line) according to the first embodiment. In addition, FIG. 8 illustrates matched waveforms of the output voltage of the light receiving circuit when the bypass circuit 40 and the voltage generation circuit 50 are removed from the light receiving circuit 10b. In the light receiving circuit in which the bypass circuit 40 and the voltage generation circuit 50 are removed and only the limiter circuit 30 operates, the frequency of a polarity is changed at the time of operation of the limiter circuit 30, and an oscillation waveform is observed (graph of dashed line). In contrast to this, the light receiving circuit 10b according to the present embodiment to which the bypass circuit 40 and the voltage generation circuit 50 are added outputs a stable waveform. In pulse characteristics of FIG. 8, the power supply voltage Vdd is set to 1.8 V, and resistance values of the feedback resistor elements 14 and 114 are set to 50 kW. In addition, a maximum output current of the light receiving element 11 is set to 25 mA, and a capacitance between terminals is set to 10 pF.

[0077]

In this way, the light receiving circuit 10b according to the present embodiment has the following effects, in addition to an effect of the light receiving circuit according to another embodiment described above. That is, the light receiving circuit 10b prevents saturation of an output waveform compared to the output current of the light receiving element 11, and thus when a signal with a large amplitude pulse is input, it is possible to obtain a more appropriate output voltage waveform with a small distortion. In addition, when an operation in which the power supply voltage is lowered is performed, an amplitude of a pulse signal which is input becomes relatively large. However, in the light receiving circuit 10b according to the present embodiment, a MOS transistor is maintained so as to operate in a saturation region from a minimum output voltage to a maximum output voltage, and thus a dynamic range of an output is secured and a low voltage operation can be performed.

Fourth Embodiment

[0078]

FIG. 9 is a circuit diagram illustrating a light receiving circuit according to a fourth embodiment.

A light receiving circuit 10c according to the present embodiment is different from the light receiving circuit 10 according to the first embodiment in that the light receiving circuit 10c includes a gate ground amplification circuit 70 which is coupled between the drain electrode 1c of the amplification transistor 1 and the internal output node 19. Hereinafter, the same symbols or reference numerals will be attached to the same circuit elements and coupling as those of the light receiving circuit 10 according to the first embodiment, and detailed description thereof will be omitted.

[0079]

The gate ground amplification circuit 70 includes a cascade transistor 7 (second MOS transistor), and bias power supply 72. The bias power supply 72 is coupled to the reference potential Vss, and supplies the gate ground amplification circuit 70 with an appropriate DC bias. The cascade transistor 7 includes a gate electrode 7a which is coupled to the bias power supply 72, a source terminal 7b which is coupled to the drain electrode 1c of the amplification transistor 1, and a drain electrode 7c which is coupled to the internal output node 19. The gate ground amplification circuit 70 is coupled to the drain electrode 1c of the amplification transistor 1 with a low impedance, and is coupled to the internal output node 19 with a high impedance. For this reason, the gate ground amplification circuit 70 can reduce a mirror capacitance of the amplification transistor 1, and thus it is possible to improve frequency characteristics of the amplification circuit which includes the amplification transistor 1, the gate ground amplification circuit 70, and the load circuit 12. In order to increase communication speed of optical communication, implementing of a broad band of a light receiving circuit is essential, and by using the gate ground amplification circuit 70, it is possible to implement a broad band of a light receiving circuit. According to the light receiving circuit 10c according to the present embodiment, by using the gate ground amplification circuit 70, a broad band of the light receiving circuit 10c can be implemented, a low voltage operation can be performed, and a dynamic range of an output is widened.

[0080]

In the same manner as the light receiving circuit 10 according to the present embodiment, the light receiving circuit 10c according to the present embodiment need to satisfy the following conditions, in order to widen the dynamic range of an output by securing a low side level of the dynamic range.

[0081]

A gate-source voltage of the amplification transistor 1 is referred to as Vgs1, a gate-source voltage of the output transistor 2 is referred to as Vgs2, and a threshold voltage and a gate-source voltage of the cascade transistor 7 are respectively referred to as Vth7 and Vgs7. In addition, if drain voltages at the time of moving from saturation regions of the amplification transistor 1 and the cascade transistor 7 to linear regions are respectively referred to as Vov1 and Vov7, and a voltage value of the bias power supply (first power supply) 72 of the gate of the cascade transistor 7 is referred to as V72 (V7), the following representation is possible.

[0082]

To begin with, from a condition in which a drain-source voltage Vov7 is satisfied when the cascade transistor 7 moves from a saturation region to a linear region, the following expressions are obtained.

Vgs1-Vgs2-(V72-Vgs7)³Vov7

\ Vgs1+Vth7-V72³Vgs2 (4)

[0083]

In addition, from a condition in which a drain-source voltage Vov1 is satisfied when the amplification transistor 1 moves from a saturation region to a linear region, the following expression is obtained.

V72-Vgs7³Vov1 (5)

By satisfying expression (4) and expression (5) in the same time, the amplification transistor 1 and the cascade transistor 7 do not deviate from a saturation region, and the light receiving circuit 10c can output a low side output voltage level.

[0084]

As described above, light receiving circuit 10c according to the present embodiment has the following effect in addition to the effect of the light receiving circuit according to another embodiment described above. That is, by cascode-coupling the gate ground amplification circuit 70 to the amplification transistor 1, a mirror capacitance of the amplification transistor 1 is decreased, and thus the light receiving circuit 10c according to the present embodiment can realize a broad band.

[0085]

By applying the gate ground amplification circuit 70 which is used for the light receiving circuit 10c according to the present embodiment to the light receiving circuit 10b according to the third embodiment, a broad band of a received signal can be implemented.

[0086]

As described above, it is preferable that the amplification transistor 1 and the cascade transistor 7 operate in a saturation region. However, if waveform distortion of the output voltage Vout of the light receiving circuit 10c is sufficiently small or there is no distortion, one or both of the amplification transistor 1 and the cascade transistor 7 may not necessarily operate in the saturation region, in the same manner as in a case of the first embodiment or the like.

Fifth Embodiment

[0087]

FIG. 10A is a block diagram illustrating an optical coupling device according to a fifth embodiment. FIG. 10B is a sectional diagram illustrating a structure of the optical coupling device according to the fifth embodiment.

The light receiving circuit according to the respective embodiments described above is used together with a light transmitting circuit which transmits an optical signal, and can be used as an optical coupling device 210. The optical coupling device 210 is used in environment or the like in which a signal transmission is hardly performed by directly coupling electrical circuits to each other due to a different voltage level between an input and an output. The optical coupling device 210 is, for example, a photocoupler.

[0088]

As illustrated in FIG. 10A, the optical coupling device 210 according to the present embodiment includes a light emitting element 211 and a receiving circuit 212.

[0089]

The light emitting element 211 is an infrared light emitting diode which includes, for example AlGaAs or the like. The light emitting element 211 is driven by a drive circuit 214. The drive circuit 214 is coupled to an external power supply which outputs a voltage of, for example, Vdd1-Vss1, and a signal is input from a signal input terminal IN. The light emitting element 211 emits light according to an input signal, and transmits an optical signal to the light receiving circuit 10. Vdd1 is, for example, +5 V, and Vss1 is, for example, -5 V.

[0090]

The receiving circuit 212 includes the light receiving circuit 10 according to the first embodiment described above. Of course, a light receiving circuit according to another embodiment may be used according to a transmission band or the like. The light receiving circuit 10 converts a received optical signal into a current using a light receiving element 11, and the current is converted into a voltage by a transimpedance amplification circuit TIA which includes an amplification circuit that is configured by the amplification transistor 1, the load circuit 12, the output transistor 2, and the load circuit 13, and the feedback resistor element 14, and is output (FIG. 1). The receiving circuit 212 may further include a waveform shaping circuit 213. The waveform shaping circuit 213 is coupled to an output of the light receiving circuit 10. The waveform shaping circuit 213 includes a comparator having, for example, a predetermined threshold voltage. The waveform shaping circuit 213 compares an analog voltage signal which is output from the light receiving circuit 10 with a threshold voltage, and thereby the analog voltage signal is converted into a digital signal and the digital signal is output from an output terminal OUT. It is preferable that the light receiving circuit 10 and the waveform shaping circuit 213 operate using a common power supply, and an operation voltage is Vdd2-Vss2. Vdd2 is, for example, 3.3 V, and Vss2 is, for example, 0 V.

[0091]

As illustrated in FIG. 10B, the optical coupling device 210 includes lead frames 221 and 222. A light emitting element chip 211a in which the light emitting element 211 is formed on a semiconductor substrate is mounted on the lead frame 221, and is coupled to the lead frame 221 by a bonding wire (not illustrated). A receiving circuit chip 212a in which the receiving circuit 212 is formed on the semiconductor substrate is mounted on the lead frame 222, and is coupled to the lead frame 222 by a bonding wire (not illustrated). The lead frames 221 and 222 are disposed in such a manner that surfaces on which the light emitting element chip 211a and the receiving circuit chip 212a are mounted face each other. Portions, which are disposed so as to face each other, of the light emitting element chip 211a and the receiving circuit chip212a are covered by a transparent resin 223 in which optical transmission loss is considered. Furthermore, peripheral portions of the portions are sealed by epoxy-based light-shielding resin 224 using, for example, a transfer mold technology. The optical coupling device 210 is electrically coupled to the drive circuit 214, using a lead of the lead frame 221 on which the light emitting element 211a is mounted, and obtains an output signal from a lead of the lead frame 222 on which the receiving circuit chip 212a is mounted.

[0092]

The optical coupling device 210 operates using a low voltage, and includes the light receiving circuit 10 with a wide dynamic range. Thus, the optical coupling device 210 can perform transmission of a signal with a low power consumption under an environment which is electrically insulated, over a wide dynamic range.

Sixth Embodiment

[0093]

FIG. 11 is a block diagram illustrating an optical communication system according to a sixth embodiment.

The light receiving circuit 10 according to the embodiments described above is used together with a transmission circuit which transmits an optical signal, and can be used as an optical communication system 230. The optical communication system 230 receives an optical signal which is transmitted via an optical fiber, converts the optical signal into an electrical signal, and outputs the electrical signal.

[0094]

The optical communication system 230 according to the present embodiment includes a transmission device 231, an optical fiber 235, and a receiving device 240. The transmission device 231 includes a drive circuit 232, and a light emitting element 233 which is driven by the drive circuit 232. The light emitting element 233 of the transmission device 231 is optically coupled to the optical fiber 235 by one end of the optical fiber 235, and transmits an optical signal. The receiving device 240 includes the light receiving circuit 10, and a waveform shaping circuit 242 which converts an analog signal output from the light receiving circuit 10 into a digital signal. The other end of the optical fiber 235 is optically coupled to the light receiving element 11 of the light receiving circuit 10 of the receiving device 240, and the light receiving circuit 10 receives an optical signal which is transmitted via the optical fiber 235. The light receiving circuit 10 converts an optical signal into an analog electrical signal and output the electrical signal to the waveform shaping circuit 242.

[0095]

The optical communication system 230 according to the present embodiment operates using a low voltage, and includes the light receiving circuit 10 with a wide dynamic range, and thus an increase of power consumption is suppressed, a communication distance can be lengthened, an optical signal is received with a high gain even if transmission loss of a transmission path is large, and the optical communication system can perform a stable operation.

[0096]

In all the embodiments described above, a light receiving circuit can be configured using a MOS transistor with polarity opposite to the MOS transistor which is illustrated.

[0097]

According to the embodiments described above, it is possible to realize a light receiving circuit and an optical coupling device which can perform a low voltage operation and perform a stable operation over a wide dynamic range.

[0098]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A light receiving circuit comprising:

a light receiving element;

a first MOS transistor of a first conductive type that includes a first gate electrode which is coupled to the light receiving element, a first source electrode which is coupled to a reference potential line, and a first drain electrode which is coupled to a first load circuit via a first node, and can operate in a saturation region;

a second MOS transistor of a second conductive type that includes a second gate electrode which is coupled to the first node, a second source electrode which is coupled to an output terminal, and a second drain electrode which is coupled to the reference potential line;

a second load circuit that is coupled between a power supply potential line and the second drain electrode; and

a feedback resistor element that is coupled between the first gate electrode and the output terminal.

2. The circuit according to Claim 1, further comprising:

a third MOS transistor that includes a third gate electrode which is coupled to the output terminal, a third source electrode which is coupled to the first gate electrode, and a third drain electrode;

a voltage generation circuit that generates a voltage equal to a voltage which is generated on the first node at the time of no signal; and

a fourth MOS transistor that is coupled between the first node and the voltage generation circuit, and includes a fourth gate electrode and a fourth drain electrode which are coupled to each other.

3. The circuit according to Claim 2,

wherein the voltage generation circuit includes,

a third load circuit, one end of which is coupled to the power supply potential line;

a fifth MOS transistor of the first conductive type that includes a fifth gate electrode which is coupled to the other end of the third load circuit, a fifth source electrode which is coupled to the reference potential line, and a fifth drain electrode which is coupled to the fourth source electrode; and

a sixth MOS transistor of the second conductive type that includes a sixth gate electrode and a sixth drain electrode which are coupled to the fifth drain electrode, and a sixth source electrode which is coupled to the fifth gate electrode.

4. The circuit according to any one of Claims 1 to 3, further comprising:

a gate ground amplification circuit that is coupled between the first drain electrode and the first node.

5. The circuit according to Claim 4,

Wherein the gate ground amplification circuit includes,

a first power supply; and

a seventh MOS transistor of the first conductive type that includes a seventh gate electrode which is coupled to an output of the first power supply, a seventh source electrode which is coupled to the first drain electrode, and a seventh drain electrode which is coupled to the first node,

wherein, when a voltage between the first gate electrode and the first source electrode is referred to as Vgs1, a threshold voltage of the first MOS transistor is referred to as Vth1, a voltage between the second gate electrode and the second source electrode is referred to as Vgs2, a voltage between the seventh gate electrode and the seventh source electrode is referred to as Vgs7, a threshold voltage of the seventh MOS transistor is referred to as Vth7, an output voltage of the first power supply is referred to as V7, and a voltage difference between Vgs1 and Vth1 is referred to as Vov1, a relationship of Vgs1+Vth7-V7³Vgs2 and V7-Vgs7³Vov1 is satisfied.

6. The circuit according to any one of Claims 1 to 3, wherein a voltage between the second gate electrode and the second source electrode is equal to or less than a threshold voltage of the first MOS transistor.

7. The circuit according to any one of Claims 1 to 6, further comprising:

A second power supply which is coupled in such a manner that a forward bias is applied between the second source electrode and a back gate electrode.

8. A light receiving circuit comprising:

a light receiving element;

a first MOS transistor of a first conductive type that includes a first gate electrode which is coupled to the light receiving element, a first source electrode which is coupled to a reference potential line, and a first drain electrode which is coupled to a first load circuit via a first node;

a second MOS transistor of a second conductive type which includes a second gate electrode that is coupled to the first node, a second source electrode that is coupled to an output terminal, and a second drain electrode that is coupled to the reference potential line, and in which a voltage between the second gate electrode and the second source electrode is equal to or less than a threshold voltage of the first MOS transistor;

a second load circuit that is coupled between a power supply potential line and the second drain electrode; and

a feedback resistor element that is coupled between the first gate electrode and the output terminal.

9. An optical coupling device comprising:

a light emitting element;

a light receiving element that receives light which is emitted from the light emitting device;

a first MOS transistor of a first conductive type that includes a first gate electrode which is coupled to the light receiving element, a first source electrode which is coupled to a reference potential line, and a first drain electrode which is coupled to a first load circuit via a first node;

a second MOS transistor of a second conductive type that includes a second gate electrode which is coupled to the first node, a second source electrode which is coupled to an output terminal, and a second drain electrode which is coupled to the reference potential line;

a second load circuit that is coupled between a power supply potential line and the second drain electrode; and

a feedback resistor element that is coupled between the first gate electrode and the output terminal.

ABSTRACT

According to one embodiment, a light receiving circuit includes a light receiving element; a first MOS transistor of a first conductive type that includes a first gate electrode which is coupled to the light receiving element, a first source electrode which is coupled to a reference potential line, and a first drain electrode which is coupled to a first load circuit via a first node, and can operate in a saturation region; a second MOS transistor of a second conductive type that includes a second gate electrode which is coupled to the first node, a second source electrode which is coupled to an output terminal, and a second drain electrode which is coupled to the reference potential line; a second load circuit that is coupled between a power supply potential line and the second drain electrode; and a feedback resistor element that is coupled between the first gate electrode and the output terminal.

DRAWINGS

FIG. 4A

TRANSIMPEDANCE (dBW)

FREQUENCY (Hz)

FIG. 4B

TRANSIMPEDANCE (dBW)

FREQUENCY (Hz)

FIG. 5

VOLTAGE (V)

TIME (ns)

PD CURRENT

PD CURRENT (mA)

- LIGHT RECEIVING CIRCUIT 10 ACCORDING TO AN EMBODIMENT

… LIGHT RECEIVING CIRCUIT 100 OF A COMPARISON EXAMPLE

FIG. 8

VOLAGE (V)

TIME (ns)

PD CURRENT

PD CURRENT (mA)

- LIGHT RECEIVING CIRCUIT 10b

… LIGHT RECEIVING CIRCUIT 10b (WITHOUT BYPASS CIRCUIT OR THE LIKE)

-×- LIGHT RECEIVING CIRCUIT 10